

#19 1/15/24

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANT'S REPLY BRIEF ON APPEAL **UNDER 37 CFR §1.193**

APPLICANT:

Stefan PFAB

DOCKET NO:

P00,0365

SERIAL NO.:

09/486,908

ART UNIT:

2186

FILED:

May 11, 2000

EXAMINER:

M. Anderson

TITLE:

DATA STORAGE DEVICE WITH OVERLAPPED BUFFERING

SCHEME

RECEIVED

Mail Stop Appeal Brief-Patents Commissioner for Patents PO Box 1450 10 Alexandria, VA 22313-1450

DEC 0 3 2003

Technology Center 2100

Sir:

In accordance with the provisions of 37 C.F.R. §1.193, Appellant submits 15 this Reply Brief in response to the Examiner's Answer, mailed September 26, 2003 and in support of the appeal of the above-referenced application for the patentability of claims 1-7 and 9-14 finally rejected in the Final Office Action (FOA), dated April 4, 2003.

PRO FORMA MATTER

DEC 0 3 2003 20 The Examiner's Answer and all other papers in this file out to the correct address of Schiff Hardin (although the last name should be "Waite" and not "White"). However, on the last page (8) of the Examiner's Answer, the name and address of an old law firm, Hill & Simpson, appears. Appellant requests that references to this address on future correspondence be 25 removed to eliminate the possibility of confusion.

NEW ISSUE RAISED IN EXAMINER'S ANSWER

In the Examiner's Answer on page 6, in the last full paragraph and the last carryover paragraph, the Examiner states that it is proper for the "data storage device" of the claims in the appeal to be read on by the combination of <u>both</u>

5 Pawlowski's main memory module 18 [or, technically, 14] and I/O module 24, and not *just* the main memory module 18 [14]. Appellant respectfully asserts that not only is this viewpoint inconsistent with how one of ordinary skill in the art would interpret a "data storage *device*", but is also inconsistent with the Examiner's own perspective in the FOA rejection. Appellant notes that this is a newly raised 10 perspective that was not brought out in any of the office actions nor in the

In the Examiner's Answer, on page 6 in the last carryover paragraph, the Examiner states that he:

| 15 | believes that the overly broad term data storage device does not limit the scope to merely the storage medium itself, but could also incorporate other elements involved in the storage of data, especially in |
|----|--|
| 20 | light of the "comprising" language in the preamble The Examine [sic] believes it is reasonable to consider Pawlowski's I/O module as part of the "data storage device" because the data output request initiated by the peripheral includes a command line portion which controls the data transfer (see column 12 lines 0.25) |
| 25 | controls the data transfer (see column 12, lines 9-25). These command line controls are essential to the data output request as they control the actual transfer of retrieved data back to the peripheral, while the system bus between the I/O module and main memory module does not include this command line portion of the full peripheral request. |

telephone interview.

30

Appellant acknowledges that an established tenet of claim construction is

that the Examiner is permitted to give claims their broadest reasonable interpretation consistent with the specification. MPEP §2111, citing *in re Hyatt*, 211 F.3d 1367, 1372 (Fed. Cir., 2000). Appellant believes, however, it is not reasonable that one of ordinary skill in the art would construe a "data storage device" as including a main memory module, an I/O module separated from the main memory module, and a bus in between to permit communication between the two entities.

In Pawlowski, the main memory 14 and the I/O module 24 are units that work independently from one another and cannot be regarded as a unit

10 representing a data storage <u>device</u>. The I/O module 24 of Pawlowski is nothing more than a bus bridge that connects the system bus 16 and the I/O bus 26. It is a mechanism via which different units connected to the system bus 16 can be accessed by the units connected to the I/O bus 26 (see Pawlowski at 5/61-65). There is no requirement that an access to the main memory 14 occurs via the I/O module 24; in fact, the CPU 12 must access the main memory 14 without using the I/O module 24. The I/O module 24 and the storage device (main memory module 14) of Pawlowski are repeatedly discussed as separate and distinct entities throughout the specification, and nowhere is it suggested that the I/O module provides a role in the storage of data.

This distinction is so clearly defined to one of ordinary skill in the art that the Examiner himself used it all previous office actions, including the FOA upon which this appeal is based.

In the FOA, page 3, under numbered paragraph 7, the Examiner states:

With respect to claims 1 and 9, Pawlowski discloses a data storage device (main memory) (see column 4, lines 5-15)... wherein the storage device (main memory) responds to a data output request...

5

Again, in the FOA, page 4, under numbered paragraph 8:

Pawlowski discloses a the [sic] selected output start address... is determined utilizing address data... applied to the data storage device (main memory)...

10

Under numbered paragraph 9:

...the selected output start address is determined by further utilizing adaptation data (data retriever) applied to the data storage (main memory)...

15

And finally, under numbered paragraph 12:

...is an address that is represented by the address data (peripheral device) applied to the data storage device (main memory)...

20

Thus, the Examiner has relied on one interpretation of the data storage device (as Pawlowski's main memory) during the prosecution of the application, and now relies on a different, and contrary to the plain and ordinary meaning, interpretation of the data storage device (as Pawlowski's main memory, plus the I/O module) for the purposes of the appeal.

Furthermore, in addition to the plain meaning of the term "data storage device", the term itself is defined in the Specification as being a "program memory", and not some aggregation of computer component devices.

As noted in MPEP §2111.01 (citing *In re Zletz*, 893 F.2d 319, 321 (Fed. 30 Cir. 1989):

During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification.

5

The originally filed Specification defines the term "data storage device" by stating, on page 2, lines 17-21:

10

Due to the slight mutual spacings of the selectable output start addresses, an output start address-leaving a few exceptions out of consideration-can always be applied with which the data representing a command can be read out from the program memory (the data storage device) on the basis of a single access.

15

Clearly, the Specification is defining the entity "data storage device" requiring the response to the data request as being the program memory, and not an aggregation of entities in a computer system. The Specification goes on to 20 state (p. 3, lines 11-14)

Tb - J-4- -

The data storage devices described in greater detail below are semiconductor memories accommodated in an integrated circuit, RAMs, ROMs, EPROMs, flash-EPROMs or the like employed as program memories to be more precise

25

While it is true that the Specification states (p. 3, lines 14, 15), "however, the data storage devices can also fundamentally be a matter of other, arbitrary storage devices", this language would be understood by one of ordinary skill in the art as still requiring some form of an integrated device—the language was added to accommodate other fabrication techniques and semiconductor materials

that might be developed throughout the life of the patent, but certainly not to aggregate any or all components of a computer system. This understanding is particularly highlighted where the Specification (page 2, top carryover paragraph) states:

In such cases [where a program memory is asked to output more data than is completely contained in response to a data output request], two read accesses onto the program memory are required... The present invention is therefore based on the object of finding a measure with which the offering of data that represent successor commands after branches or the like can be speeded up.

Although it is not proper to read the specification description as limitations

15 in the claims *per se*, one would certainly not understand the specification's

definition of the term "data storage device" to permit the inclusion of an additional intervening (and thus, speed reducing) element that would make the very same problematic multiple requests of the program memory as provided in the prior art.

In the Examiner's Answer, page 6, third paragraph, the Examiner states,

"However, it is noted that these features upon which applicant rely are not recited in the rejected claims". Appellant believes this feature, by use of the phrase "data storage device" given its plain and ordinary meaning, given its meaning as understood by the Examiner throughout the prosecution of the application, and given its meaning as defined in the specification, is, in fact, recited in the claims

25 for the reasons explained above.

CONCLUSION

For the above reasons, Appellants respectfully submits that the Examiner is in error in law and in fact in rejecting claims 1-7 and 9-14 based on the teachings of the above-discussed reference.

5 Reversal of the rejection of all of those claims is justified, and the same is respectfully requested.

Appellant believes that no additional fee is due, but, if necessary, the Commissioner is hereby authorized to charge any additional fees which may be required to account No. 50-1519.

Respectfully submitted,

Mark Bergner
SCHIFF HARDIN & WAITE

Patent Department
6600 Sears Tower
233 South Wacker Drive
Chicago, Illinois 60606-6473
Customer Number: 26574
(312) 258-5779
Attorneys for Appellant

CERTIFICATE OF MAILING

I hereby certify that an original and two copies of this correspondence are being deposited with the United States Postal Service as First Class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on November 26, 2003.

30

Mark Bergner – Attorney for Appellant